IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 12-15, 20, 22, 23 and 25 without prejudice or disclaimer.

Please AMEND claims 1, 11, 21 and 24 in accordance with the following:

1. (CURRENTLY AMENDED) A method for provisionally determining quantity and positions of a plurality of power supply pads when designing a semiconductor integrated circuit including a core section provided with a plurality of nodes and the plurality of power supply pads, with each power supply pad being connected to the core section via an IO buffer, wherein each IO buffer has a predetermined current capacity, the method comprising:

performing a power supply network analysis of the core section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculating current values of the power supply pads from the calculated current values between the nodes;

determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer; ~~and~~

eliminating or adding at least one power supply pad in accordance with the result of the determination; and

eliminating at least one power supply pad when the current value of each of the power supply pads does not exceed the current capacity of the associated IO buffer.

2. (ORIGINAL) The method according to claim 1, wherein said calculating voltage values of the nodes includes calculating IR drop values between the nodes based on the voltage value of each node and suspending subsequent processing when any one of the calculated IR drop values exceeds a predetermined maximum IR drop value.

3. (ORIGINAL) The method according to claim 1, wherein said performing a power

supply network analysis includes modeling the core section as a plurality of equivalent circuits electrically equivalent to one another, each equivalent circuit including a resistor and a current source, and performing the power supply network analysis on the modeled core section.

4. (ORIGINAL) The method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power supply wire density in the core section.

5. (ORIGINAL) The method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power consumption of the core section.

6. (ORIGINAL) The method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of the current values of the power supply pads.

7. (ORIGINAL) The method according to claim 1, wherein the designed semiconductor integrated circuit is provided with a plurality of pads including the power supply pads, the method further comprising:

initially defining all of the pads as power supply pads at which the potential is the same,

wherein said eliminating or adding at least one power supply pad includes eliminating a power supply pad of which current value is less than the current capacity.

8. (ORIGINAL) The method according to claim 7, further comprising:

determining whether a completion condition is satisfied after deleting the at least one power supply pad, wherein subsequent processing is terminated when the completion condition is satisfied, and said performing a power supply network analysis is executed again when the completion condition is not satisfied.

9. (ORIGINAL) The method according to claim 7, wherein said initially defining all of the pads includes selecting from all of the power supply pads a power supply pad that has a determined location to use the selected power supply pad as a reference pad, said eliminating or adding at least one power supply pad includes checking whether deletion of every one of the power supply pads excluding the reference pad is possible.

10. (ORIGINAL) The method according to claim 9, wherein said eliminating or adding at least one power supply pad includes distributing the current value of one power supply node, excluding the reference pad, at a predetermined ratio to the reference pad, comparing the current value of the reference pad subsequent to the distribution with the current capacity, and determining whether deletion of the power supply is possible in accordance with the comparison result.

11. (CURRENTLY AMENDED) A method for provisionally determining quantity and positions of a plurality of power supply pads before detailed design of a semiconductor integrated circuit, wherein the semiconductor integrated circuit includes a core section provided with a plurality of nodes and a plurality of power supply pads, the method comprising:

initially defining all of the pads as power supply pads at which the potential is the same;

performing a power supply network analysis of the core section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculating current values of the power supply pads from the calculated current values between the nodes;

determining whether there is a power supply pad for which current value is less than or equal to a predetermined current capacity; ~~and~~

adding a new power supply pad near a power supply pad for which current value exceeds the predetermined current capacity, and assigning a power supply pad as another type of pad when the current value of that power supply pad is less than or equal to the predetermined current capacity; and

eliminating at least one power supply pad when the current value of each of the power supply pads does not exceed the current capacity of the associated IO buffer.

12. (CANCELLED)

13. (CANCELLED)

14. (CANCELLED)

15. (CANCELLED)

16. (CANCELLED)

17. (CANCELLED)

18. (CANCELLED)

19. (CANCELLED)

20. (CANCELLED)

21. (CURRENTLY AMENDED) An apparatus for designing a semiconductor integrated circuit including a core section provided with a plurality of nodes and a plurality of power supply pads, the core section having a plurality of nets, each including a plurality of wires, each power supply pad being connected to the core section via an IO buffer, wherein each IO buffer has a current capacity, the apparatus comprising:

a storage device which stores power consumption information of the core section and power supply wire resistance information, including resistances between the nodes; and

a data processor in communication with the storage device, in which the data processor:

performs a power supply network analysis of the core section by referring to the power consumption information and the power supply wire resistance information to calculate voltage values of the nodes[[;]],

calculates current values between the nodes from the voltage values of the nodes and the resistances between the nodes[[;]],

calculates current values of the power supply pads from the calculated current values between the nodes[[;]],

determines whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer~~; and~~,

eliminates or adding a power supply pad in accordance with the result of the determination to determine the quantity and locations of the power supply pads, and

eliminates at least one power supply pad when the current value of each of the power supply pads does not exceed the current capacity of the associated IO buffer.

22. (CANCELLED)

23. (CANCELLED)

24. (CURRENTLY AMENDED) A recording medium comprising computer instructions stored thereon for determining quantity and positions of a plurality of power supply pads in a semiconductor integrated circuit including a core section provided with a plurality of nodes, each power supply pad being connected to the core section via an IO buffer, wherein each IO buffer has a predetermined current capacity, the computer instructions when executed by a computer performing steps including:

carrying out a power supply network analysis of the core section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculating current values of the power supply pads from the calculated current values between the nodes;

determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer; ~~and~~

eliminating or adding at least one power supply pad in accordance with the result of the determination; and

eliminating at least one power supply pad when the current value of each of the power supply pads does not exceed the current capacity of the associated IO buffer.

25. (CANCELLED)